THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

April 21, 2004

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE.

APPLICATION NUMBER: *60/444,987*
FILING DATE: *February 04, 2003*
RELATED PCT APPLICATION NUMBER: *PCT/US04/03170*

By Authority of the
COMMISSIONER OF PATENTS AND TRADEMARKS

T. Wallace
T. WALLACE
Certifying Officer

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

02-06-03 ... 02044 Prov #

Certificate of Mailing byExpress Mail

In accordance with the provisions of 37 CFR 1.10, I hereby certify that the attached was deposited with the U.S. Postal Service for delivery by Express Mail on February 4, 2003. The number of the Express Mail mailing label is: EL 897 961 972 US.

Signed: _____

Name: Michael K. Kinney Registration No. 42,740

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).
EXPRESS MAILING LABEL No.: EL 897 961 972 US

Docket No. 102441-100			Type a plus (+) Inside this box 6	+
INVENTOR(s)/APPLICANT(s)				
LAST NAME	FIRST NAME	MIDDLE INITIAL	RESIDENCE (CITY AND EITHER STATE OR FOREIGN COUNTRY)	
JUSKEY	FRANK	J.	PLEASANTON, CA	
LAU	DANIEL	K.	SAN FRANCISCO, CA	

TITLE OF INVENTION (280 characters max)

THIN MULTIPLE SEMICONDUCTOR DIE PACKAGE

CORRESPONDENCE ADDRESS

Customer Number:

27267
PATENT TRADEMARK OFFICE

Enclosed Application Parts (check all that apply)

[X] Specification (claims & abstract)	Number of pages [8]	
[X] Drawing(s)	Number of Sheets [7]	[X] Other (specify) ___ Self-addressed, prepaid return receipt postcard _X_

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT (check one)

[ ] A check or money order is enclosed to cover the filing fees
[...] Applicant claims small entity status. See 37 CFR 1.76.
[X] The Commissioner is hereby authorized to charge filing fees and credit Deposit Account No. 23-1665

Filing Fee Amount(s) $ $160.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

[X] No [ ] Yes, the name of the U.S. Government agency and the Government contract number is _____.

Respectfully submitted,

SIGNATURE: _____ Date: February 4, 2003

TYPED or PRINTED NAME: Michael K. Kinney Registration No. 42,740

Telephone: 203-498-4411

\14587\2\357539.1

THIN MULTIPLE SEMICONDUCTOR DIE PACKAGE

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates generally to semiconductor manufacture and, more particularly, to the packaging of a multiple semiconductor die package.

2. DESCRIPTION OF PRIOR ART

Portable electronic devices such as, for example, radiotelephones, pagers and personal electronic assistants (PDAs), are becoming increasingly complex, while also being provided in increasingly smaller and lighter form factors. Semiconductor chips or dice such as, for example a microprocessor die and a memory die, are used within the portable electronic devices. Typically, a die is provided in a ceramic or plastic packaging that provides support, protection, dissipates heat for the die and provides a lead system for power and signal distribution. One type of packaging provides individually packaged dies. Another type of packaging provides many dies in one package.

One example of a package having multiple semiconductor dice is U.S. Patent No. 6,452,278, issued September 17, 2002, to Vincent DiCaprio et al. DiCaprio et al. describe a package including a substrate having a central aperture. DiCaprio et al. further describe one or more semiconductor dice disposed within the aperture to provide a thin profile.

As is appreciated by those in the art, there are higher costs associated with reworking a failure in packages including multiple dies as opposed to reworking a failed, single die package. To minimize cost, semiconductor manufacturing employs a Known Good Die (KGD) rule. Generally speaking, the KGD rule refers to a die level product provided by a semiconductor die manufacturer that carries with it a certain level of guaranteed reliability.

Accordingly, the inventors realized that a need exists for semiconductor packages having higher functionality (e.g., more than one die in a package), a thin profile and which satisfy the KGD rule.

BRIEF DESCRIPTION OF THE DRAWINGS

The above set forth and other features of the invention are made more apparent in the ensuing Detailed Description of the Preferred Embodiments when read in conjunction with the attached Drawings, wherein:

FIG. 1A is a plan view of a support structure for a semiconductor die package including a lead frame and a carrier;

FIG. 1B is a side, cross-sectional view of the semiconductor die package support structure of FIG. 1A;

FIG. 2A is a plan view of the support structure of FIG. 1A with semiconductor dies attached therein;

FIG. 2B is a side, cross-sectional view of the semiconductor die package support structure of FIG. 2A;

FIG. 3A is a plan view of the support structure of FIG. 2A illustrating a molding operation;

FIG. 3B is a side, cross-sectional view of the semiconductor die package of FIG. 3A;

FIG. 4A is a plan view of the support structure of FIG. 3A illustrating removal of a carrier portion of the support structure;

FIG. 4B is a side, cross-sectional view of the semiconductor die package of FIG. 4A;

FIG. 5A is a plan view of the support structure of FIG. 4A illustrating forming of fingers of the lead frame;

FIG. 5B is a side, cross-sectional view of the semiconductor die package of FIG. 5A;

FIGS. 6A and 6B illustrates exemplary features of one embodiment of a semiconductor die package constructed in accordance with the present invention; and

FIG. 7 illustrates an exemplary stacked multiple semiconductor die assembly constructed in accordance with one embodiment of the present invention.

Identically labeled elements appearing in different ones of the above-described figures are intended to refer to the same elements but may not be referenced in the description for all figures.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGS. 1A and1B illustrate a support structure for a semiconductor die package including a lead frame 10 dispose on a carrier 20 such as, for example, a thin tape or laminate. In accordance with one aspect of the present invention, the lead frame 10 is configured as a plurality of rows and columns to accommodate a plurality of semiconductor dice in apertures in the lead frame, shown generally at 12, formed between associated intersections of the rows and columns. In one embodiment, the carrier 20 is a thin tape made of polyimide or another plastic material.

As shown in FIGS. 2A and 2B, a plurality of semiconductor dice 30 are positioned within the lead frame 10, e.g., in the apertures 12 formed at the intersections of associated rows and columns. Each of the dice includes a first surface 32 and a second surface 34. Wire bonds 40 are disposed on the first surface 32 of each die 30 to electrically couple the die 30 to the lead frame 10. The carrier 20 supports the second surface 34 of the die 30. It should be appreciated that each of the plurality of semiconductor dice 30 are disposed in the apertures 12 formed between intersections of the rows and columns of the lead frame 10 such that the first surface 32 of each die 30 is substantially coplanar with a first surface 14 of the lead frame 10.

As shown in FIGS. 3A and 3B, an encapsulant 50 is individually molded over each of the plurality of dice 30 and wire bonds 40 such that the encapsulant 50 substantially encompasses each of the dice 30, e.g., by filling corresponding apertures 12. In one embodiment, sides of the encapsulant 50 are tapered.

Once the encapsulant 50 is applied to the lead frame 10, the carrier 20 may be removed. FIGS. 4A and 4B, illustrate the removal operation. When complete, the plurality of dice 30 are suspended within the apertures 12 of the lead frame 10 by the encapsulant 50. The first surface 32 of each die 30 is encapsulated while the second surface 34 is exposed.

FIGS. 5A and 5B illustrate an individual semiconductor die package, shown generally at 100, that has been separated from the lead frame strip. As shown in FIGS. 5A and 5B, exposed portions of the lead frame 10 define fingers 10' that are formed in an "s-like" shape. The fingers 10' extend down from the first surface 14 of the lead frame and provide a cavity, shown generally at 102, below the die 30. Once separated, the die packages 100 are tested and burned-in in accordance with industry

standard processes to ensure KGD reliability.

FIGS. 6A and 6B illustrates one embodiment of the semiconductor die package 100 configured in accordance with the present invention. Three exemplary dimensions are labeled "A", "B" and "C" and illustrate thickness of the package 100. As shown, the novel configuration of the package 100 facilitates formation of stacked, multiple semiconductor die packages having a thin profile.

For example, FIG. 7 illustrates a five semiconductor die package 200 wherein layered die packages 210-250, respectively, are assembled. It should be appreciated that each of the die packages 210-250 are similar to die package 100, except that dimensions A of corresponding lead frame FINGERS 10' vary to accommodate lower level packages. As shown in FIG. 7, the die packages 210-250 and corresponding lead frame portions are such that as the die package 200 is assembled, the encapsulated die and wire bonds of a lower die package is positioned in a cavity (e.g., similar to cavity 102) formed by a next higher stacked die package in the assembly 200. For example, die package 210 is assembled such that disposed within cavity 222 of die package 220, die package 220 is disposed within cavity 232 of die package 230, die package 230 is disposed within cavity 242 of die package 240 and die package 240 is disposed within cavity 252 of die package 250.

It should be appreciated that the relative thickness of the die package 200 is calculated by tally successive sets of the A, B and C, or B and C dimensions of the associated die packages 210-250 as follows.

First Layer - die package 210, thickness = A + B + C; plus

Second Layer – die package 220, thickness = B + C (since dimension A is already accounted for by the lower layer); plus

Third Layer – die package 230, thickness = B + C; plus

Fourth Layer – die package 240, thickness = B + C; plus

Fifth Layer – die package 250, thickness = B + C.

Accordingly, stacked die packages assembled as shown with respect to die package 200 realize a thinner profile than conventional stacked die packages wherein each die package is simple assembled upon a lower level package.

It should also be appreciated that FIGS. 1A-5B depict exemplary stages of assembly of a stacked semiconductor package, such as that shown in FIG. 7.

Some benefits of stacked semiconductor packages configured in accordance with the present invention include:

- The package is an ideal KGD and stacked die package solution for less than about 200 I/O;
- Using a lead frame instead of laminate substrate reduces the cost of the package;
- Recessing a die such that it is substantially flush to surrounding lead frame portions allows a low profile package of about 0.4mm thickness.

While the invention has been described and illustrated in connection with preferred embodiments, many variations and modifications, as will be apparent to those of skill in the art, may be made without departing from the spirit and scope of the invention. By example, and as discussed above, the teachings of this invention are not intended to be limited to any specific number of stacked die package arrangement, such as the five die package arrangement described in detail above. That is, it should be appreciated that aspects of the present invention apply equally to other semiconductor arrangements where a thinner profile is desirable.

Accordingly, the invention as set forth in the appended clams is not limited to the precise details of construction set forth above as such other variations and modifications as would be apparent to one skilled in the art are intended to be included within the spirit and scope of the invention as set forth in the defined claims.

CLAIMS

What is claimed is:

1. A stacked semiconductor die assembly, comprising:

a plurality of die packages, each including:

a lead frame having an aperture, a first surface and a plurality of fingers extending down from said first surface to form a cavity below said lead frame;

a semiconductor die disposed in the aperture, said semiconductor die having a first surface and a second surface, said first surface being substantially coplanar with said first surface of said lead frame;

a plurality of wire bonds electrically coupling said semiconductor die to said lead frame; and

an encapsulant disposed in said aperture and substantially encompassing said semiconductor die and said plurality of wire bonds, said second surface of said semiconductor die being exposed to said cavity;

wherein said plurality of die packages are assembled in a layered manner such that said encapsulated semiconductor die and wire bonds are disposed in said cavity of a next higher die package in said layered assembly.

2. A method for forming a stacked multiple semiconductor die assembly, comprising:

forming a plurality of individual semiconductor die packages, including:

providing a support structure including a lead frame disposed on a

carrier, the lead frame having a plurality of rows and columns and apertures formed at intersections of the plurality rows and columns;

attaching a plurality of semiconductor dice to the carrier within the apertures of the lead frame such that a first surface of each semiconductor die is substantially coplanar with a first surface of the lead frame;

electrically coupling each of the semiconductor dice to the lead frame with a plurality of wire bonds;

individually encapsulating each of the semiconductor die and wire bonds such that the apertures is filled;

removing the carrier from the lead frame to expose a second surface of the semiconductor, the second surface being opposite to the first surface of the semiconductor; and

forming a plurality of fingers from portions of the lead frame extending from the aperture and down from the first surface of the lead frame, the fingers forming a cavity below the aperture; and

forming a multiple semiconductor die assembly in a layered manner by disposing a first semiconductor die package in the cavity formed by the fingers of a next higher semiconductor die package.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for forming a multiple semiconductor die assembly having a thin profile are presented. The assembly includes one or more individually formed semiconductor packages stacked in a layered manner. Each semiconductor package includes a lead frame, a semiconductor die electrically coupled to the lead frame by wire bonds. The lead frame has an aperture, a first surface and a plurality of fingers extending down from the first surface to form a cavity below the lead frame. The semiconductor die is disposed in the aperture and has a first surface and a second surface. The first surface is substantially coplanar with the first surface of the lead frame. An encapsulant is disposed in the aperture and substantially encompasses the semiconductor die and wire bonds, while leaving the second surface of the semiconductor die exposed to the cavity. The assembly is formed in a layered manner such that the encapsulated semiconductor die and wire bonds of a first die package are disposed in the cavity of a next higher die package in the layered assembly.

FIG. 1A

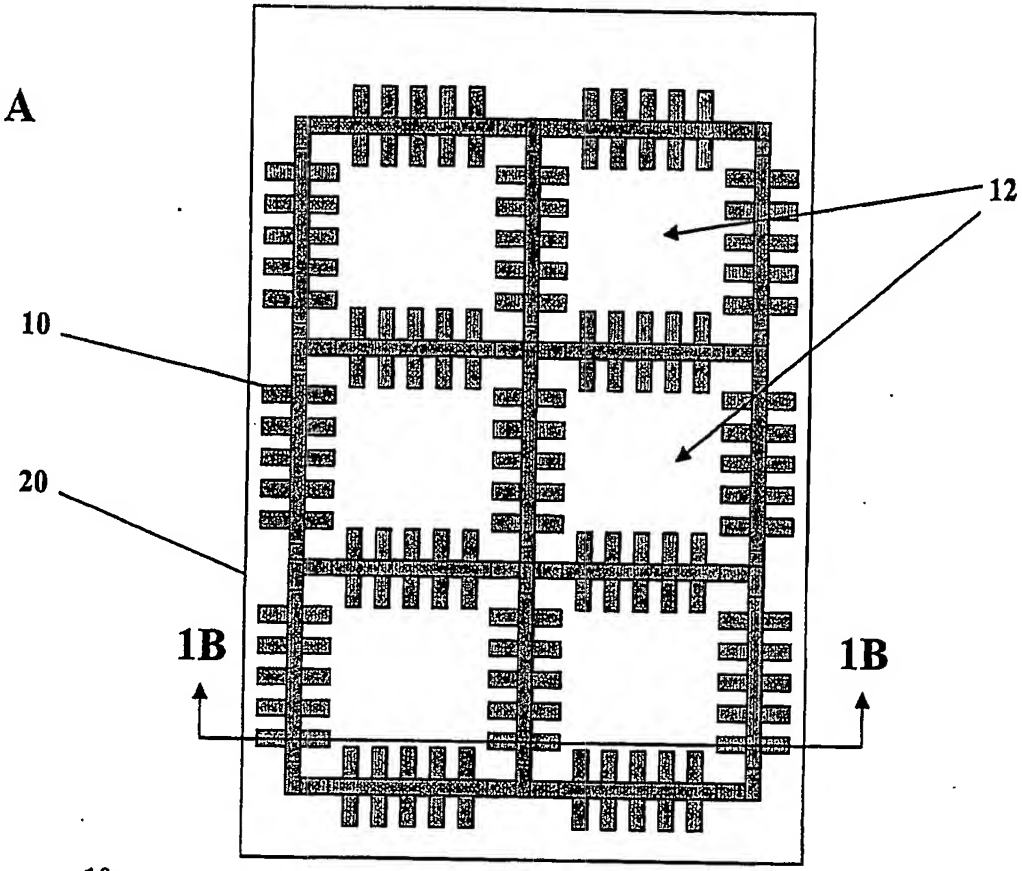
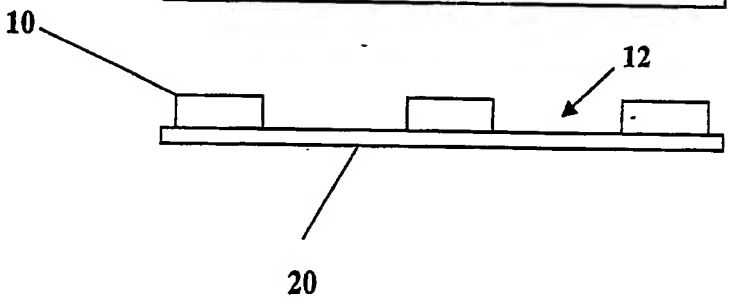


FIG. 1B



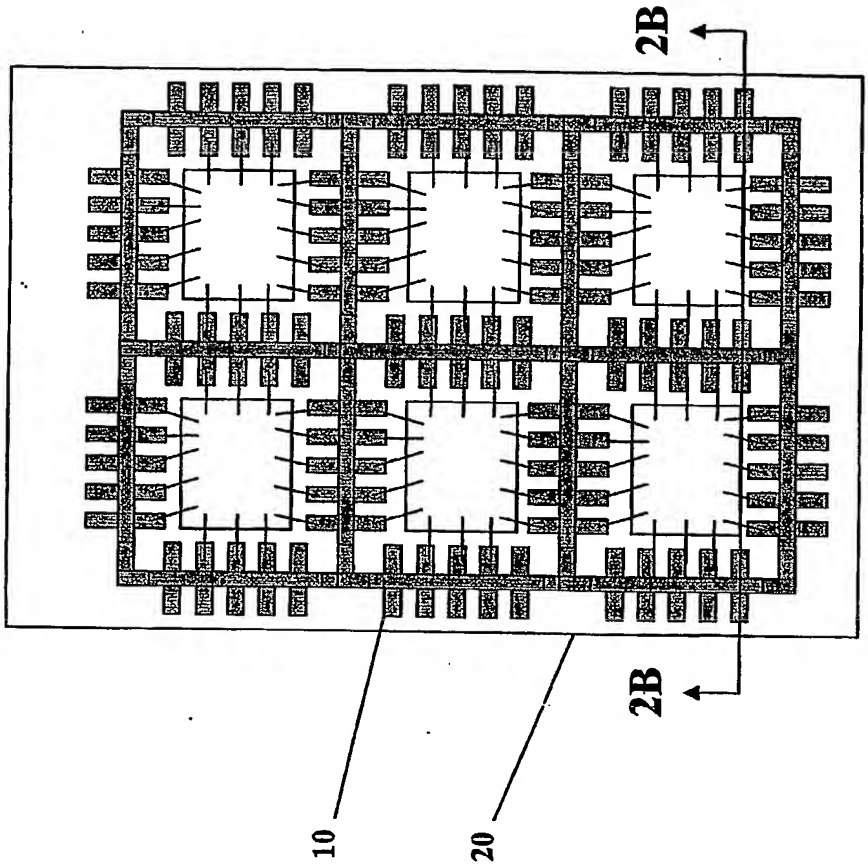


FIG. 2A

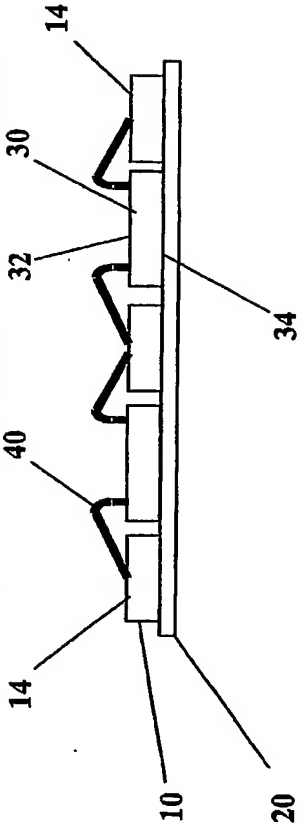


FIG. 2B

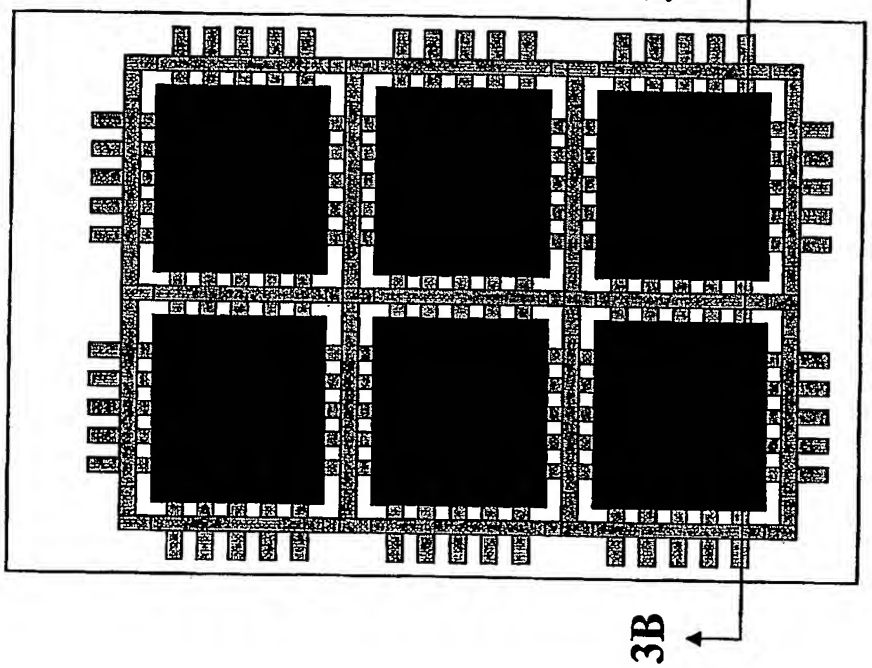


FIG. 3A

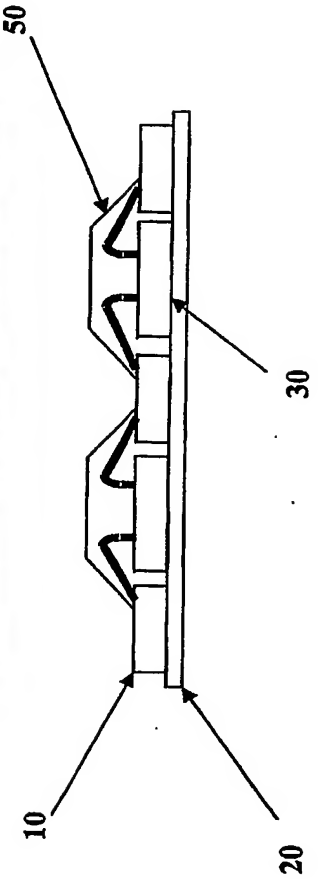


FIG. 3B

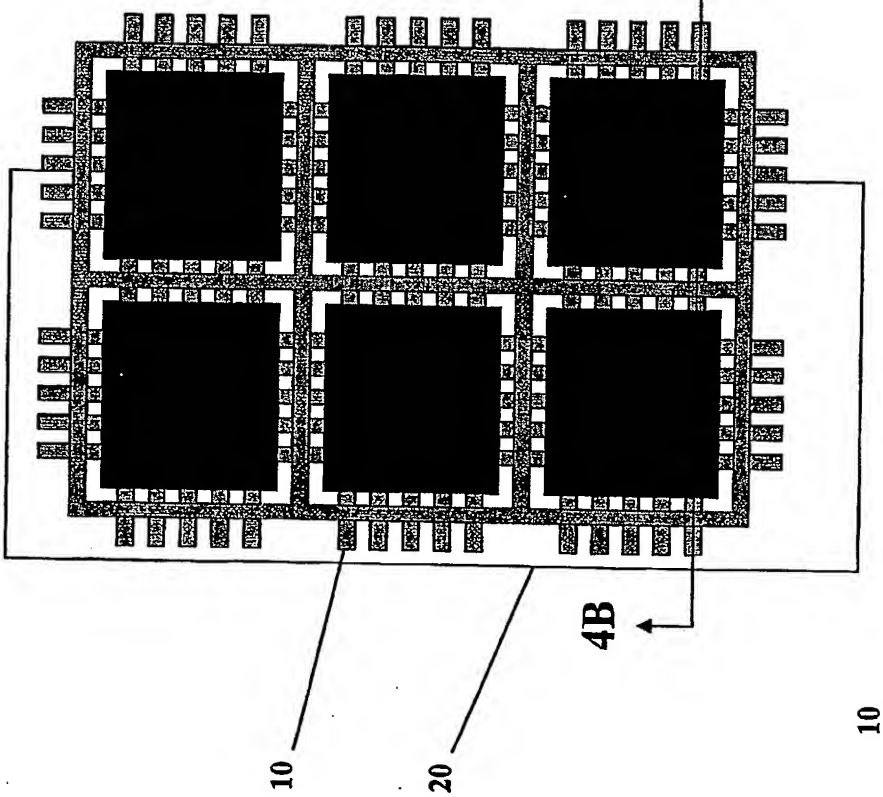


FIG. 4A

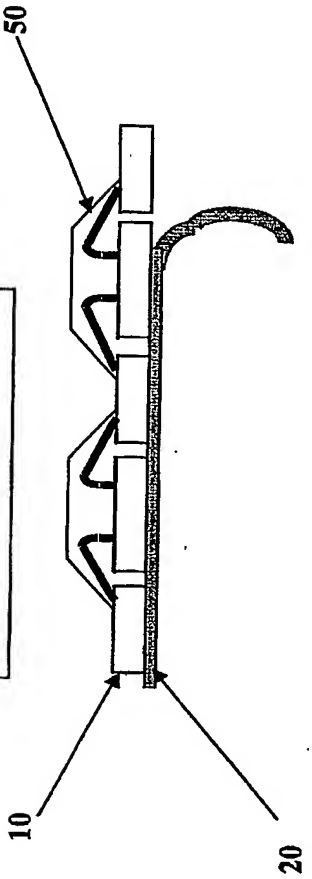


FIG. 4B

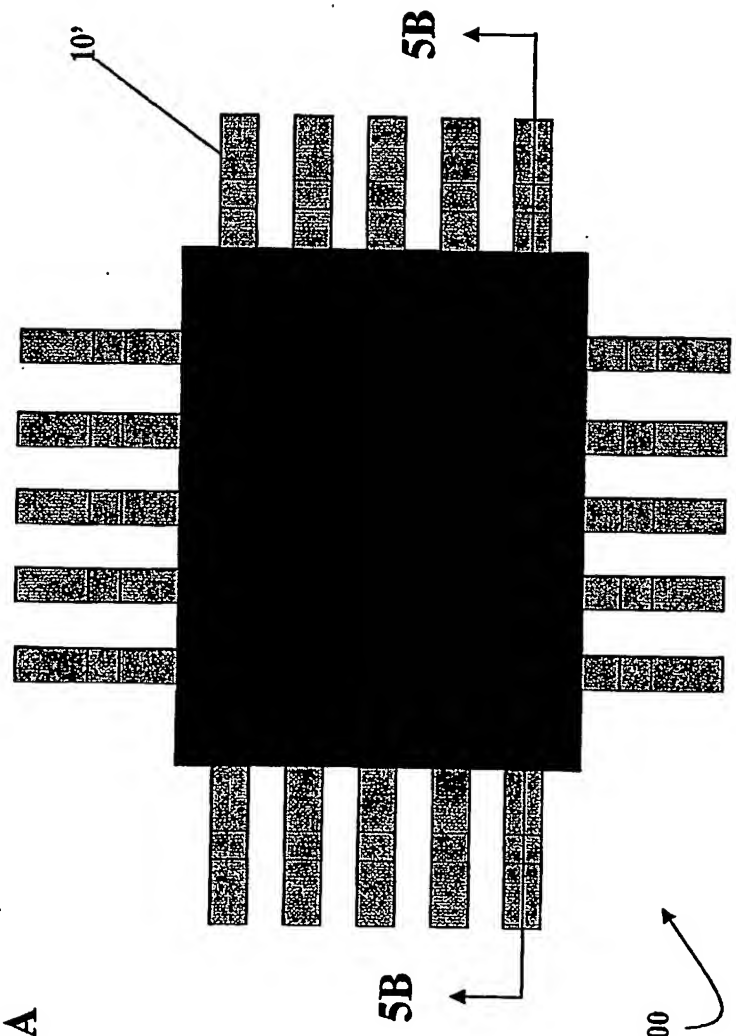


FIG. 5A

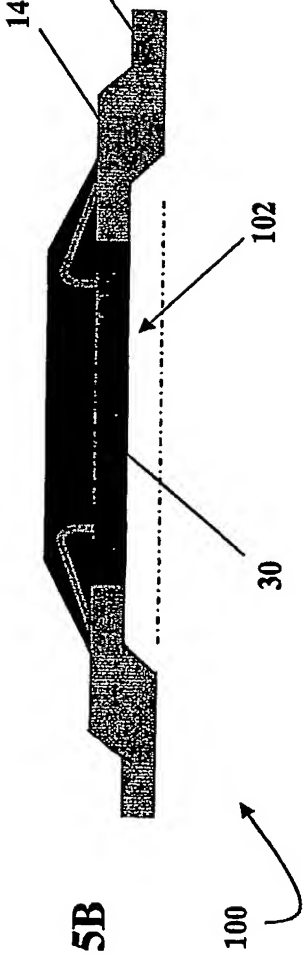


FIG. 5B

FIG. 6A

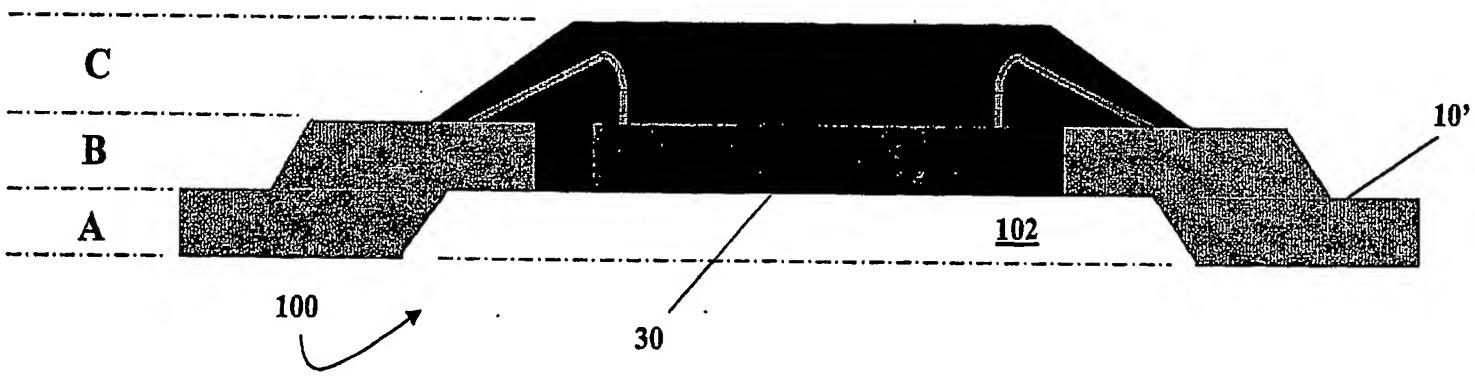


FIG. 6B

A). Lead Frame Thickness	0.200 MM	8 mils
B). Lead Frame Form	0.100 MM	4 mils
C). Mold Cap Thickness	0.250 MM	10 mils
A + B + C	0.550 MM	22 mils
B + C	0.350 MM	14 mils

FIG. 7